## REMARKS

In response to the Office Action mailed on 07/24/06, Applicant wishes to enter the following remarks for the Examiner's consideration. Applicant has cancelled claims 1-5, 8 and 9, amended claims 6, 7 and 10, and added new claims 14 and 15. Claims 1-15 are pending in the application. This response accompanies the filing of a request for continued examination (RCE).

**Rejection of claims under 35 USC §101**

Claims 1, 6 have been rejected under 35 USC §101 as being directed towards non-statutory subject matter. Applicant respectfully traverses this rejection of the claims in view of the amendment to claim 6.

Regarding claim 1, the examiner has interpreted "computer readable medium" as including a data flow graph. He also states that a data flow graph is not a tangible result because it is abstract. Applicant submits that these statements are inconsistent since an abstract entity cannot be "computer readable". Nonetheless, claim 1 and its dependent claims 2-5 have been cancelled without prejudice.

Claim 6 has been amended to describe "A method for a processor to process a sequence of a plurality of multiple-instruction control words". Claim 6 has been further amended to include the element "disabling an element of the processor, to reduce power consumption by the processor, if a corresponding bit of the identifier is set". Thus the final, useful, result is made clear: namely, the processor operates with reduced power. This feature is illustrated in FIG. 5 of the specification for example. Furthermore, this result is tangible in the sense that power consumption of a processor may be

measured. This amendment is supported by the specification on page 4, lines 3-5 and on page 6, lines 12-18, for example.

In view of the amendment to claim 6, applicant respectfully submits that the 35 USC §101 rejection of claim 6 has been overcome and requests that this basis of rejection of the claim be withdrawn and that a Notice of Allowance for this claim, and its dependents, be mailed at the Examiner's earliest convenience.

**Rejection of claims under 35 USC §102(b)**

Claims 1, 4-6 and 8-12 have been rejected under 35 USC §102(b) as being anticipated by Tanaka (Patent No. US 5,893,143). Applicant respectfully traverses this rejection of the claims.

Claims 1-5 have been cancelled without prejudice.

Claim 6 has been amended to clarify that the identifier has "one bit for each element of the processor, wherein a bit of the identifier is set if a corresponding ordered field contains a NOP instruction in every multiple-instruction control word of the sequence of control words". This amendment is supported by FIG. 1 of the specification that shows a single mask having 10 bits – one for each of the 10 datapath elements. The single mask is used for all of the control words of the sequence. This is in contrast to the Tanaka reference in which a separate bit-mask is used for each control word. For example, FIG. 6 of Tanaka shows 5 masks, one for each of the 5 control words (see 720 for example). The approach of Tanaka allows for higher compression, but requires more complex hardware for execution. In addition, more memory is required to store the bit-masks.

In amended claim 6, a bit of the identifier is set if a corresponding ordered field contains a NOP instruction in every multiple-instruction control word of the sequence of a plurality of control words. In contrast, Tanaka has a mask for each control word. Applicant submits that the mask of Tanaka is not equivalent to the identifier of claim 6.

Claim 6 has also been amended to clarify that the disabled elements remain disabled while the sequence of instructions is processed. Thus, the hardware is configured only once before processing of the sequence begins. This is in contrast to Tanaka where the hardware is reconfigured for each control word, dependent upon both bit masks and cache hits. This is disadvantageous, since the process of reconfiguration consumes processor power. However, power consumption is not a primary concern for Tanaka, since his objective is to minimize amount of cache memory used.

In Tanaka the processing element 110b in figure 12 is controlled by signal 400c. Referring to figure 11, signal 400c is a cache hit signal. This signal depends on whether an instruction has been loaded from a main memory (5 in figure 5) into an instruction cache 100a. In Tanaka, the mask information 410 is reported through signal line 410, which controls the selectors 120 – not the processing unit 110. Applicant submits that selectors 120 are not equivalent to processing elements. They may be elements of the processor, but processing is performed by the processing units 110.

Claim 6 has been further amended to specify that a sequence of control words contains a plurality of control words.

Claims 8 and 9 have been cancelled without prejudice.

Claim 10 has been amended, in a similar fashion to claim 6, to clarify

that the compression mask has "one bit for each element of the processor, wherein a bit of the identifier is set if a corresponding ordered field contains a NOP instruction in every multiple-instruction control word of the sequence of control words". Thus a single compression mask is used for the whole sequence of control words. In light of the foregoing, it is clear that the mask of Tanaka is not equivalent to the mask of claims 10-12.

Claim 10 further calls for a pipelined permute unit, coupled to the logic unit and the memory and operable to reconstruct multiple-instruction control words by fetching a compressed multiple-instruction control word from the memory and inserting NOP instructions in accordance with the compression mask. The examiner refers to Tanaka column 3, lines 6-13. However, in column 3, lines 14-33 Tanaka describes disadvantages of the use of a pipeline for parallel processing in VLIW processor. In column 6, lines 1-2 Tanaka talks about inserting a NOP into an instruction field but makes no mention of how this achieved. In particular, Tanaka does not teach or otherwise suggest the use of pipelined permute unit.

Claims 11 depends from claim 10. Claim 11 has been amended to clarify that the memory banks remain disabled while the sequence of control words is processed. The examiner opines that Tanaka disables clusters, however, these clusters are configured for every control word according to cache hits and the mask for that control word. A single mask does not select clusters for an entire sequence of control words.

Claim 12 also depends from claim 10. Claim 12 has been amended to clarify that the compression mask is used to disable processing elements of the plurality of processing elements that are unused by all control words of the

sequence of multiple-instruction control words. This amendment serves to further distinguish the claim from Tanaka, where clusters may be selected or deselected many times during the processing of a sequence of control words.

In light of the foregoing amendment and remarks, Applicant respectfully submits that the Tanaka reference does not teach, suggest, disclose or otherwise anticipate the recitations of claims 6 and 10-12. Applicant thus respectfully requests that this basis of rejection of the claims be withdrawn and that a Notice of Allowance for these claims be mailed at the Examiner's earliest convenience.

**Rejection of claims under 35 USC §103**

Claim 2 have been rejected under 35 USC §103(a) as being unpatentable over Tanaka (Patent No. US 5,893,143) in view of Mehrotra (US 6,710,016). Applicant has been cancelled claim 2 without prejudice.

Claims 3 and 13 have been rejected under 35 USC §103(a) as being unpatentable over Tanaka (Patent No. US 5,893,143) in view of Pechanek (US 6,173,389),

Claim 3 has been cancelled without prejudice.

Claim 13. The Examiner acknowledges that the Tanaka reference fails to teach, disclose or suggest the recitation of claim, and relies upon the teachings of Pechanek (US 6,173,389) to overcome this defect. Applicant respectfully traverses this rejection of the claim. Claim 13 depends from claim 10 discussed above. Both Tanaka and Pechanek treat each field value as a

short instruction word (SIW) and store the short instruction words together with information to allow the VLIW to be reconstructed. Tanaka (See figure 6 packs four SIW into the same space as a VLIW, but the field order is not maintained. Pechanek just stores the SIW. All of the approaches reduce the amount of memory required to store the instructions, however, Pechanek and Tanaka both require information on how to rebuild each VLIW (see Pechanek column 3, lines 2-4, for example). The approaches of Tanaka and Pechanek achieve high compression ratios, but they require relatively complex circuitry to rearrange the VLIW slices (the SIWs). This is because the positions of the slices of the VLIW are not maintained in the compressed representation. In claim 13, which depends from claim 10, a single compression mask is used for each sequence of control words. In a vector processor loops are often repeated many times. Having a single compression mask means that the hardware need be configured only once for the loop (for example, a processing element or memory bank may be disabled for the whole execution of the loop). This is possible since the fields containing NOPs are aligned within a sequence. In contrast, Tanaka requires a compression mask for each instruction of the loop. Pechanek does not cure this defect, since each VLIW is built up from SIWs. For example, Pechanek figure 5 teaches that each VLIW 510 includes enable mask bits (bits 10-17). The examiner maintains that Tanaka figure 6 shows that the fields are aligned, however 710 shows for example FIELD2-a is positioned in the same column as FIELD0-b, thus the 'a' fields are no longer aligned. Similarly the first column of 710 contains both 'a' fields and 'b' fields. (700 and 720 show uncompressed fields.)

Applicant submits that the one-per-sequence compression mask of claim 13 is not equivalent to one-per-word compression mask of Tanaka, nor the one-per-word enable mask bits of Pechanak.

It can be seen in light of the foregoing discussion of Pechanek reference, however, that even if one were to combine the Tanaka reference with Pechanek, the result would not be the claimed invention of claim 13.

In light of the foregoing remarks, Applicant respectfully submits that the Tanaka and Pechanek references, whether considered alone or in combination fail to teach, disclose, suggest or otherwise render obvious the recitations of claim 13. Applicant thus respectfully requests that this basis of rejection of the claim be withdrawn and that a Notice of Allowance for claim 13 be mailed at the Examiner's earliest convenience.

Claim 7 has been rejected under 35 USC §103(a) as being unpatentable over Tanaka (Patent No. US 5,893,143) in view of Shebanow (US 5,367,494).

The Examiner acknowledges that the Tanaka reference fails to teach, disclose or suggest the recitation of claim 7, and relies upon the teachings of Shebanow (US 5,367,494) to overcome this defect. Applicant respectfully traverses this rejection of the claims. Claim 7, which depends from claim 6, calls for disabling a memory bank of the plurality of memory banks while the sequence of control words is processed, to reduce power consumption by the processor further, if a corresponding bit of the identifier is set.

Referring to Tanaka figure 6, even if the main memory 710 or the cache memory 720 were banked memory (and this is not taught or otherwise suggested by Tanaka), it would have four banks, a, b, c and d. All four banks

must be enabled because the number of fields (slices) in the compressed control words 701 is the same as the number of slices in the uncompressed or decompressed control words. Even if the capability to disable memory banks were available (as taught by Shebanow), Tanaka cannot take advantage of this capability since all fields (slices) of the VLIW are in use at one time or another. Tanaka could only disable memory banks on a per-word basis, not for an entire sequence, as called for in claim 7.

In light of the foregoing remarks, Applicant respectfully submits that the Tanaka and Shebanow references, whether considered alone or in combination fail to teach, disclose, suggest or otherwise render obvious the recitations of claim 7. Applicant thus respectfully requests that this basis of rejection of the claim be withdrawn and that a Notice of Allowance for claim 7 be mailed at the Examiner's earliest convenience.

**New Claims**

Applicant has added new claims 14 and 15. Claims 14 and 15 , like claims 10-13, are structure claims. Support for claims 14 and 15 is provided by FIG. 4 and the corresponding description thereof.

Claim 14 includes a mask latch for storing a bit mask having of one bit for each datapath element, wherein a bit of the bit mask is set if a corresponding ordered field contains a NOP instruction in every multiple-instruction control word of the sequence of control words.

As discussed at length above, the bit mask describes where NOP instructions are positioned in the same fields in <u>every</u> control word of the sequence.

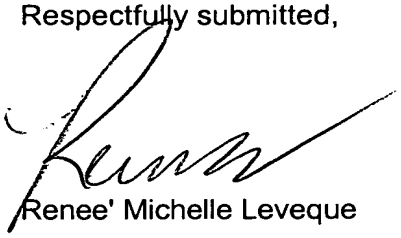
Claim 14 also calls for a logic unit coupled to the mask latch, the memory banks and the datapath elements and operable to enable and disable memory banks and datapath elements, in accordance with the bit mask, before the sequence of control words is processed. This further distinguishes the claimed system from prior systems, since the hardware is configured only at the start of a processing sequence, not on a word-by-word basis. This approach simplifies the hardware and allows for reduced power consumption.

Claim 15 depends from claim 14.

In light of the foregoing amendments and remarks, applicant submits that all rejections of claims 6, 7 and 10-13 have been overcome. The scope of the amended claims is substantially the same with implicit meaning now made explicit. Allowance of claims 6, 7, 10-13 and new claims 14 and 15 is therefore respectfully requested at the Examiner's earliest convenience. Although additional arguments could be made for the patentability of each of the claims, such arguments are believed unnecessary in view of the above discussion. The undersigned wishes to make it clear that not making such arguments at this time should not be construed as a concession or admission to any statement in the Office Action.

Please contact the undersigned if you have any questions regarding this application.

Respectfully submitted,



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